IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Presented) A method of operating a semiconductor processing system comprising:

determining a first state for a wafer via optical digital profiling using critical dimension data and sidewall angle data;

determining a second state for the wafer via optical digital profiling using critical dimension data and sidewall angle data;

determining a process recipe to change the state of the wafer from the first state to the second state;

performing the process recipe on the wafer, wherein the state of the wafer changes from the first state to a processed state;

determining when the processed state is not the second state; and

updating the process recipe.

2. (Previously Presented) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the first state further comprises measuring at least one of an electrical property and a physical property.

3. (Previously Presented) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the first state further comprises receiving at least one of electrical data and physical data.

4. (Previously Presented) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the second state further comprises measuring at least one of an electrical property and a physical property.

5. (Previously Presented) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the second state for a wafer further comprises receiving at least one of electrical data and physical data.

6. (Original) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the process recipe comprises feeding forward at least one process recipe based on the first and second state of the wafer.

7. (Original) The method of operating a semiconductor processing system as claimed in claim 1, wherein the determining of the process recipe comprises predicting the second state using the first state of the wafer and a process model based on the process conditions.

8. (Original) The method of operating a semiconductor processing system as claimed in claim 1, further comprising:

determining differences between the processed state and the second state; and

feeding back the differences.

9. (Currently Amended) A method of operating a semiconductor processing system comprising:

determining a first state for a wafer via optical digital profiling using critical dimension data and sidewall angle data;

substantially simultaneously determining a second state for the wafer via optical digital profiling using critical dimension data and sidewall angle data;

substantially simultaneously determining a predicted state for the wafer, wherein a predicted process recipe is used to change the state of the wafer from the first state to the predicted state;

substantially simultaneously determining a modeled state for the wafer, wherein a process module is used to change the state of the wafer from the first state to the modeled state;

substantially simultaneously determining a measured state for the wafer, and

determining a recipe for changing the wafer state to the second state using the first state, the predicted state, the modeled state, and the measured state.

10. (New) A method of operating a semiconductor processing system comprising:

determining a first state for a wafer via optical digital profiling using critical dimension data and sidewall angle data, wherein the determining the first state uses filtered metrology data;

determining a second state for the wafer via optical digital profiling using critical dimension data and sidewall angle data, wherein the determining the second state uses filtered metrology data;

determining a process recipe to change the state of the wafer from the first state to the second state;

performing the process recipe on the wafer, wherein the state of the wafer changes from the first state to a processed state;

determining when the processed state is not the second state; and

updating the process recipe.

11. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the first state further comprises measuring at least one of an electrical property and a physical property.

12. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the first state further comprises receiving at least one of electrical data and physical data.

13. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the second state further comprises measuring at least one of an electrical property and a physical property.

14. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the second state for a wafer further comprises receiving at least one of electrical data and physical data.

15. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the process recipe comprises feeding forward at least one process recipe based on the first and second state of the wafer.

16. (New) The method of operating a semiconductor processing system as claimed in claim 10, wherein the determining of the process recipe comprises predicting the

second state using the first state of the wafer and a process model based on the process conditions.

17. (New) The method of operating a semiconductor processing system as claimed in claim 10, further comprising:

determining differences between the processed state and the second state; and

feeding back the differences.

18. (New) A method of operating a semiconductor processing system comprising:

determining a first state for a wafer via optical digital profiling using critical dimension data and sidewall angle data, wherein determining the first state comprises measuring a bottom critical dimension in a gate stack;

determining a second state for the wafer via optical digital profiling using critical dimension data and sidewall angle data, wherein determining the second state comprises measuring a bottom critical dimension in a gate stack;

determining a process recipe to change the state of the wafer from the first state to the second state;

performing the process recipe on the wafer, wherein the state of the wafer changes from the first state to a processed state;

determining when the processed state is not the second state; and

updating the process recipe.

19. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the first state further comprises measuring at least one of an electrical property and a physical property.

20. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the first state further comprises receiving at least one of electrical data and physical data.

21. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the second state further comprises measuring at least one of an electrical property and a physical property.

22. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the second state for a wafer further comprises receiving at least one of electrical data and physical data.

23. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the process recipe comprises feeding forward at least one process recipe based on the first and second state of the wafer.

24. (New) The method of operating a semiconductor processing system as claimed in claim 18, wherein the determining of the process recipe comprises predicting the second state using the first state of the wafer and a process model based on the process conditions.

25. (New) The method of operating a semiconductor processing system as claimed in claim 18, further comprising:

determining differences between the processed state and the second state; and

feeding back the differences.